

# FPGA-Based Real-Time Simulation of Permanent Magnet Synchronous Motor Drive for Vehicular Applications

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## Extended Abstract

### Introduction

Nowadays, it is a common engineering practice to test a motor controller against a simulated motor model running in real-time before using the controller in real-life conditions. This has several advantages. For example, the simulated motor can be tested with borderline conditions that would damage a real motor, sometimes a costly prototype. The motor itself may be under development in parallel to the controller and therefore may not even be available. The controller is interfaced with the real-time simulated motor through a set of proper I/Os; this is called Hardware-In-the-Loop (HIL) simulation.

New, fast digital controller for motor drive can have very small input-output latency below 10 microseconds and therefore requires that the real-time simulated motor have a computational time much lower than this value. The reason is that the model computational time (including the I/O access times) adds a delay in the loop of the final closed-loop response of the controlled motor. If this added delay is too large compared to the real delay (a real motor has no latency), the HIL simulation may diverge from the response of the controller with a real motor.

Recently, HIL simulation of PMSM drive have been reported to run on RT-LAB with sample rate below 10 microseconds[1]. The RT-LAB real-time simulator, from Opal-RT Technologies, uses standard PCs with FPGA-based I/O board on the PCI bus. In this configuration, the main performance limitation is the relative low rate of data transfers from the PCI bus to/from the multi-GHz CPUs. FPGA-based simulation of the PMSM motor can alleviate this data transfer problem by locating the motor computational tasks just besides the I/O on the same FPGA card.

### Objective of the work

The FPGA-modeled PMSM motor drive was made with the following considerations and objectives

- The simulator must have the smallest input-output latency.
- The model must be accurate, especially with regards to the flux calculation.
- The implementation of the model should not require advanced FPGA programming techniques like VHDL.
- The PMSM model of the FPGA should come with some test capability.
- The PMSM model should be independent of motor rating and able to accept a wide variety of parameters.

- The simulator must provide an easy way to acquire data computed on the FPGA for monitoring purposes. Modifications of the model parameters from a Console PC must also be achievable easily.

At the time of writing of this paper, real-time simulation of PMSM motors on an FPGA medium have not been reported in the literature. A few papers report on FPGA-based simulation of induction motors. In [2][3], the induction motor is implemented using custom-made floating-point arithmetic for the most part. In [4], the induction motor was simulated in XSG for validation purpose but the final model was designed using VHDL language and fixed-point arithmetic. The approach described in this paper also uses XSG but is incorporated into RT-LAB, a real-time distributed simulation platform. This permits the XSG design to be directly compiled and executed on the FPGA within the RT-LAB framework.

The capability of simulating complex models like PMSM inside the FPGA core itself is a new feature of the RT-LAB real-time simulation platform (v8.0 and later). It can also be used to implements controllers and/or Firing Pulse Units.

RT-LAB enables the distributed simulation of complex electromechanical devices: part of the devices (ex: mechanical equations) can be implemented in Simulink with a Pentium chip as real-time simulation target while the PMSM model (and/or controller) can be implemented with XSG with the FPGA as target. RT-LAB will in this case manage communications between the CPUs, the FPGA and the Console PC from which the global simulation is controlled.

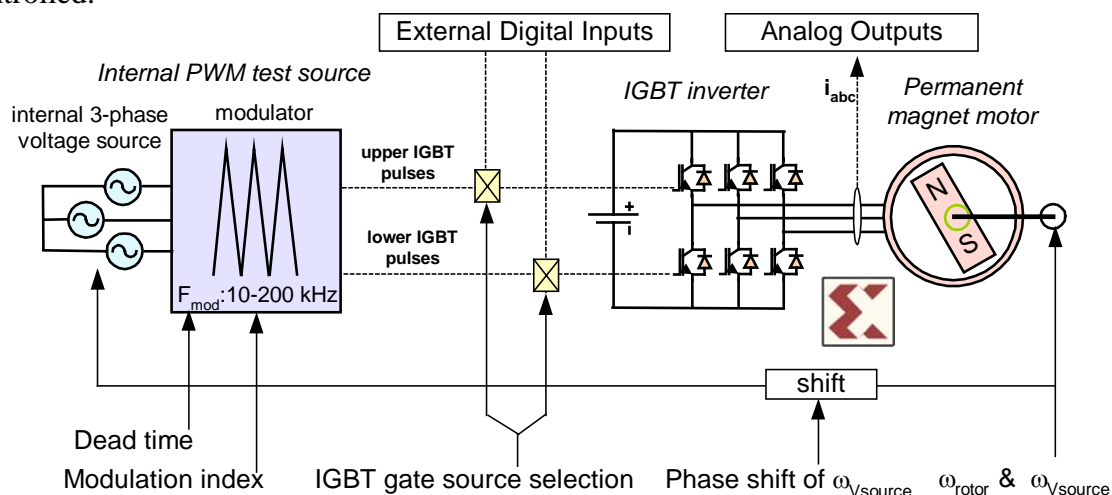


Figure 1 Xilinx System Generator PMSM drive simulated on the FPGA card

Figure 1 describes the PMSM, IGBT inverter and PWM test source that were designed in XSG and executed in RT-LAB. The stator of the PMSM is driven by a 3-phase IGBT inverter with dead time capability (10 ns resolution). The inverter IGBT gate signals can come from external I/O or by an internal PWM source. In the latter case, the modulation signal is a 3-phase sinusoidal source with the exact rotor frequency but with a user variable phase shift. The user can also modify the PWM carrier frequency of the modulator as well as its dead time. Simulation with rotor-synchronous internal PWM source therefore results in constant Park  $d$ - $q$  quantities and electrical torque. By modifying the stator PWM voltage phase shift, one can observe and study its effect on the electrical torque. Similarly, by modifying the PWM dead time, one can observe distortions on motor currents. The machine phase currents are also outputted to fast D/A with 1 microsecond conversion rate if external control is to be used.

## Validation tests

The first test (Test #1) consists on comparing the open-loop PWM steady state response of the PMSM model in XSG with a regular Simulink counterpart (from SimPowerSystems blockset). In this test, the model runs in open-loop PWM with constant phase difference between the rotor angle and the PWM input voltage, using the circuit of Figure 1. The sampling of FPGA data point was made at 2.5  $\mu$ s (250 times the 10 ns FPGA simulation sample time). The test is made with the following parameters:

Table 1. Parameters used for Test #1.

Carrier frequency	12.2 kHz
Modulation index	0.6
Dead time	1 $\mu$ s
Source angle	95 degrees
DC link voltage	300V (1 pu)

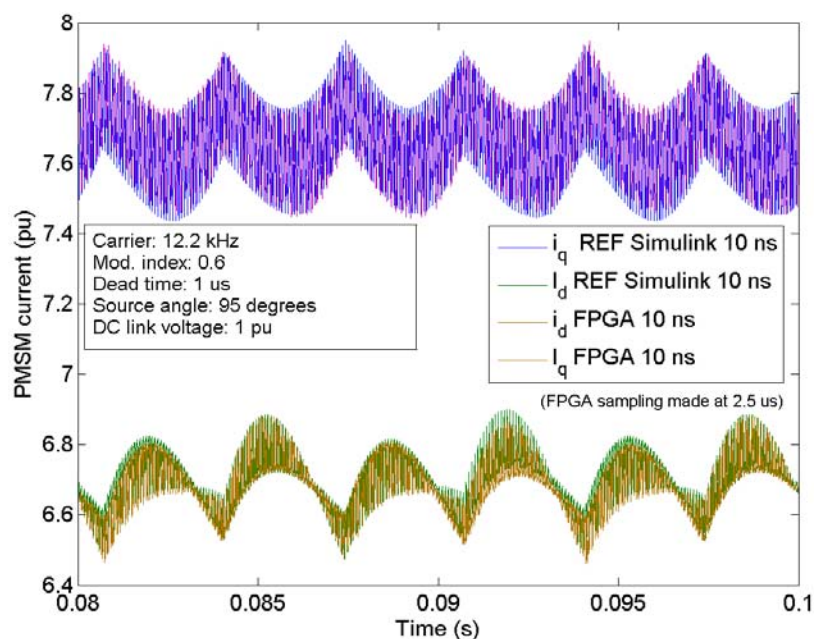


Figure 2. Test #1 results: d-q motor currents; XSG vs. Simulink at 10 ns

The curves of Figure 2 match very well. The differences can be mostly explained by the large acquisition step (decimation) in the FPGA case. It is worth noticing that the FPGA acquisition was very simply made in a Simulink interface, one of the user interface available in RT-LAB.

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